FIG.1
CONVENTIONAL ART

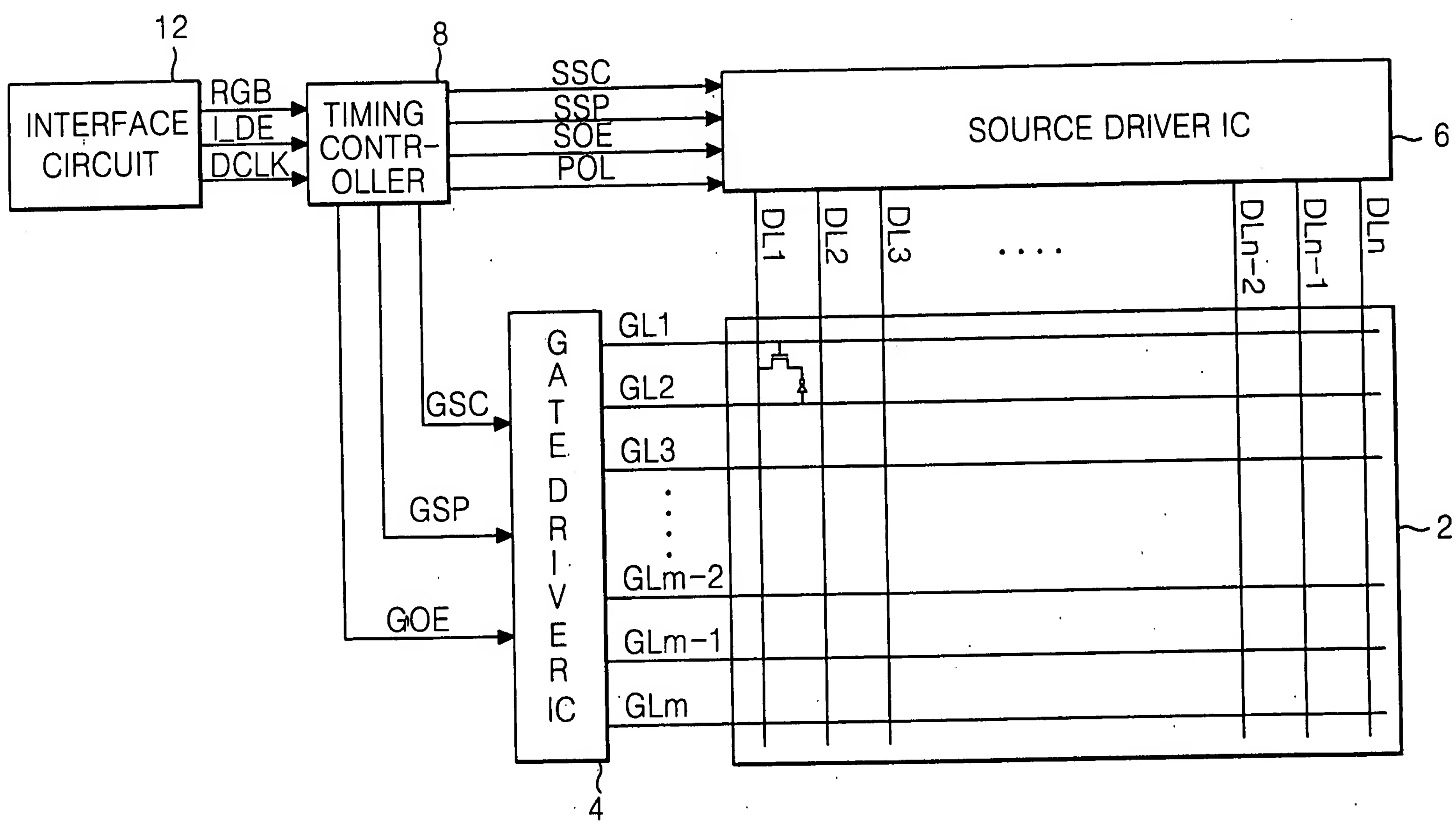

FIG.2
CONVENTIONAL ART

Video Mode	N	PinName
WHEN THE NUMBER OF DCLK AT DE BLANKING INTERVAL IS EVEN NUMBER(n)	1	Dclk [XGA: 65MHz] (Falling Edge에서 Latch)
	2	Video Data
	3	Data Lactch
	4	Toggle at Dclk Rising
	5	Odd Data La1ch
	6	FOUR TIMES Toggle SIGNAL INVERSION
	7	Even Data Latch
	8	FOUR TIMES Toggle SIGNAL INVERSION
	9	Even Data Latch
	10	FOUR TIMES Toggle SIGNAL INVERSION
	11	Even Data {D-IC INPUT Video Signal}
	12	Odd Data {D-IC INPUT Video Signal}
	13	Odd Enable
	14	SSP
WHEN THE NUMBER OF DCLK AT DE BLANKING INTERVAL IS ODD NUMBER(n+1)	15	FOUR TIMES Toggle SIGNAL INVERSION
	16	Even Data {D-IC INPUT Video Signal}
	17	Odd Data {D-IC INPUT Video Signal}
	18	Data Enable
	19	SSP

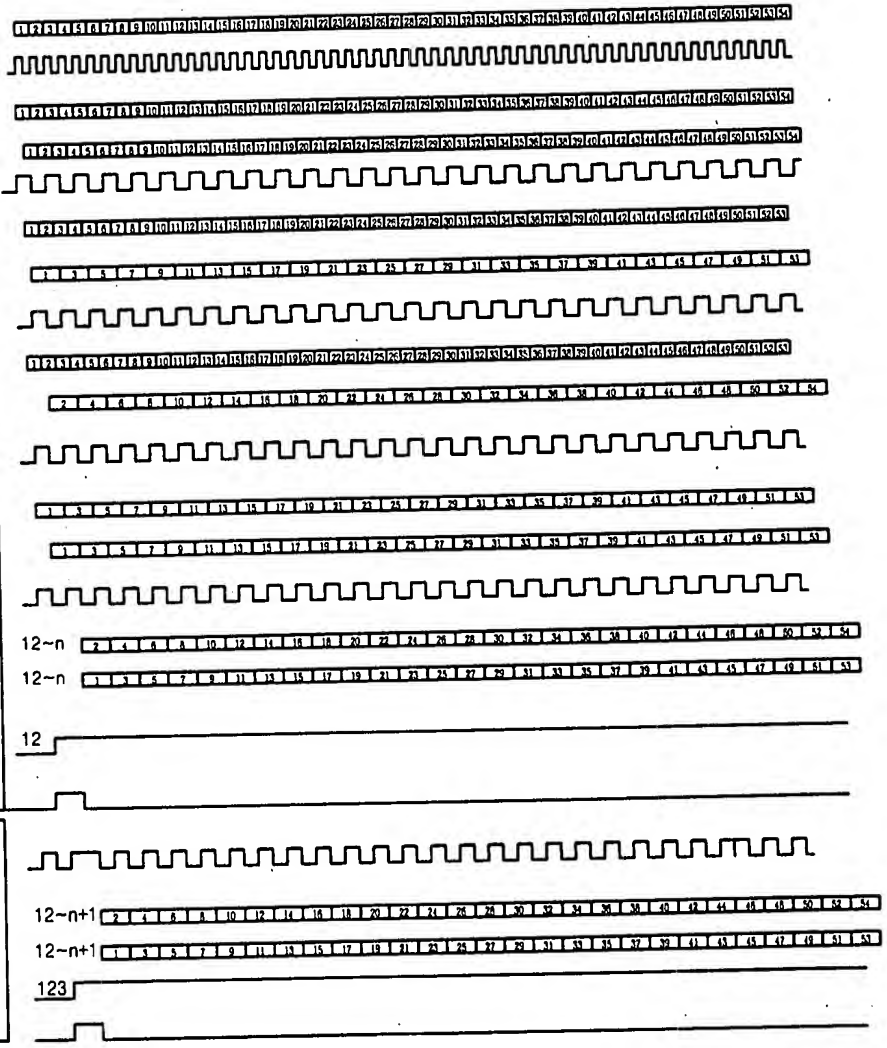

FIG.3
CONVENTIONAL ART

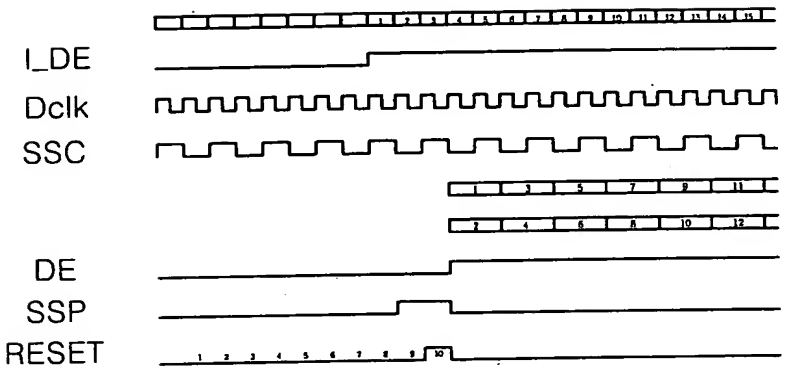

FIG.4
CONVENTIONAL ART

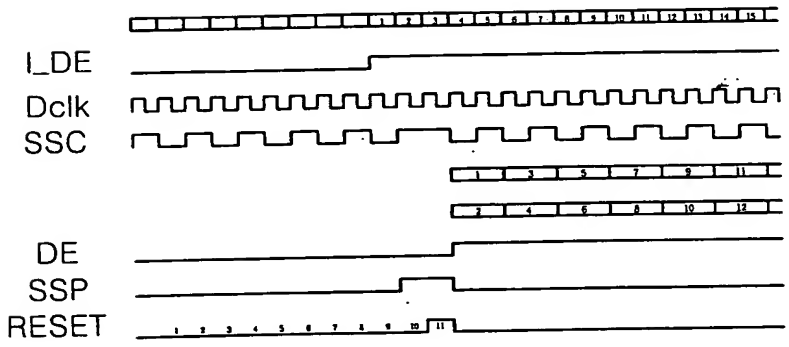

FIG.5

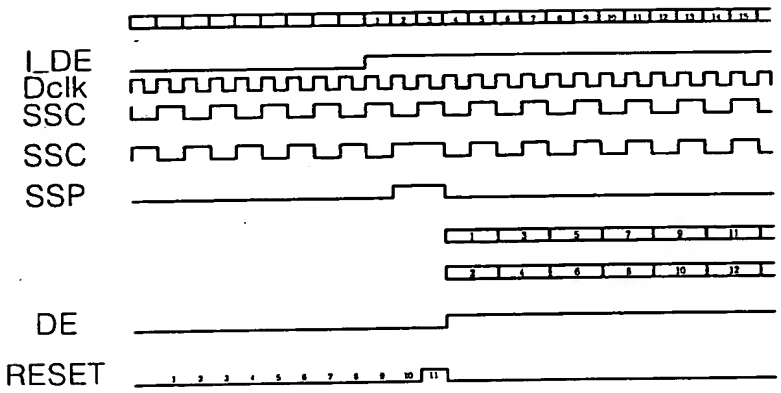

FIG.6

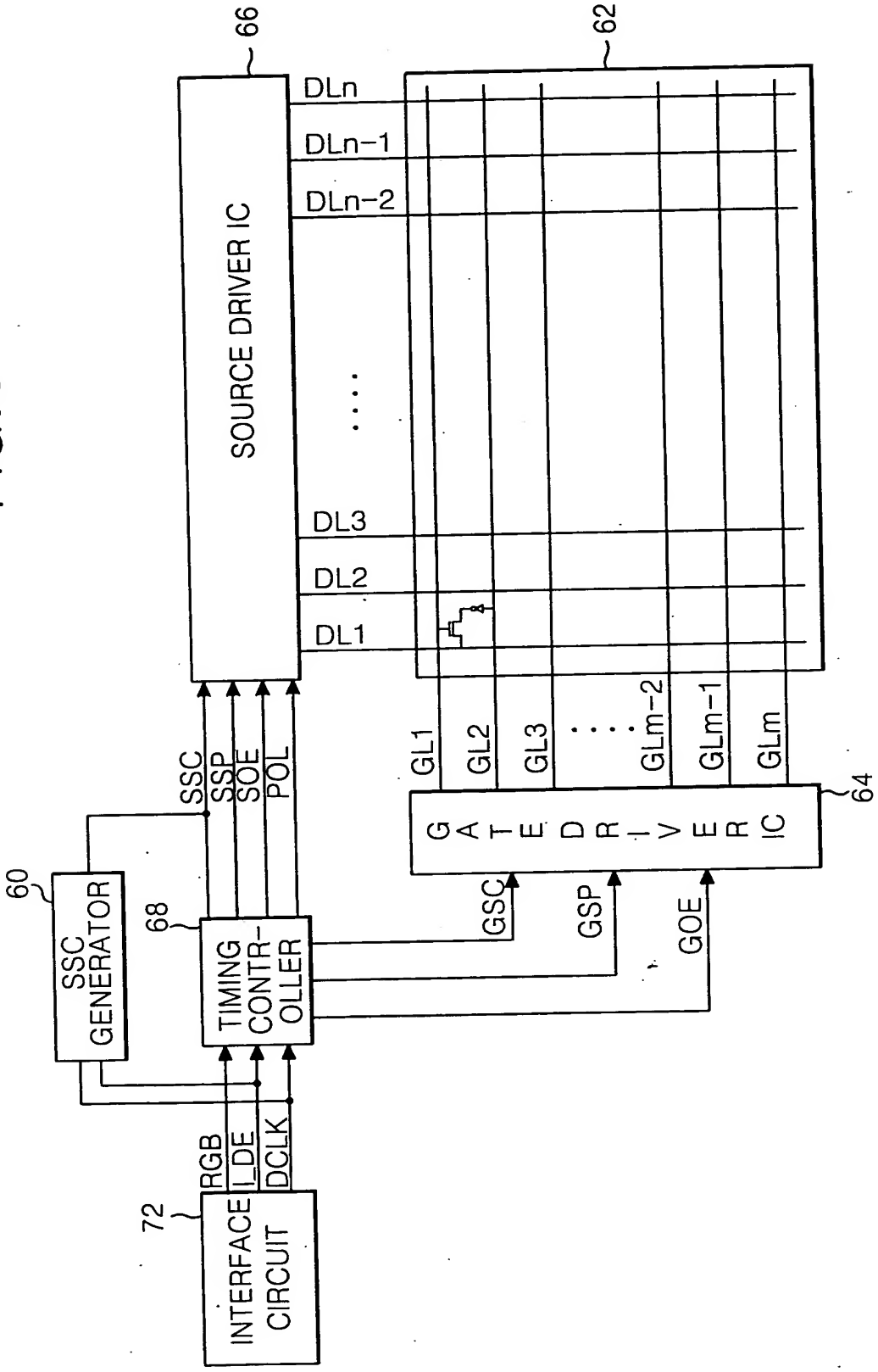
66
62
SOURCE DRIVER IC
DLn
DLn-1
DLn-2
DL3
DL2
DL1
GL1
GL2
GL3
GLm-2
GLm-1
GLm
GATE DRIVER IC
64
SSC
SSP
SOE
POL
GSC
GSP
GOE
60
SSC GENERATOR
68
TIMING CONTR-OLLER
RGB
I_DE
DCLK
72
INTERFACE CIRCUIT

FIG.7

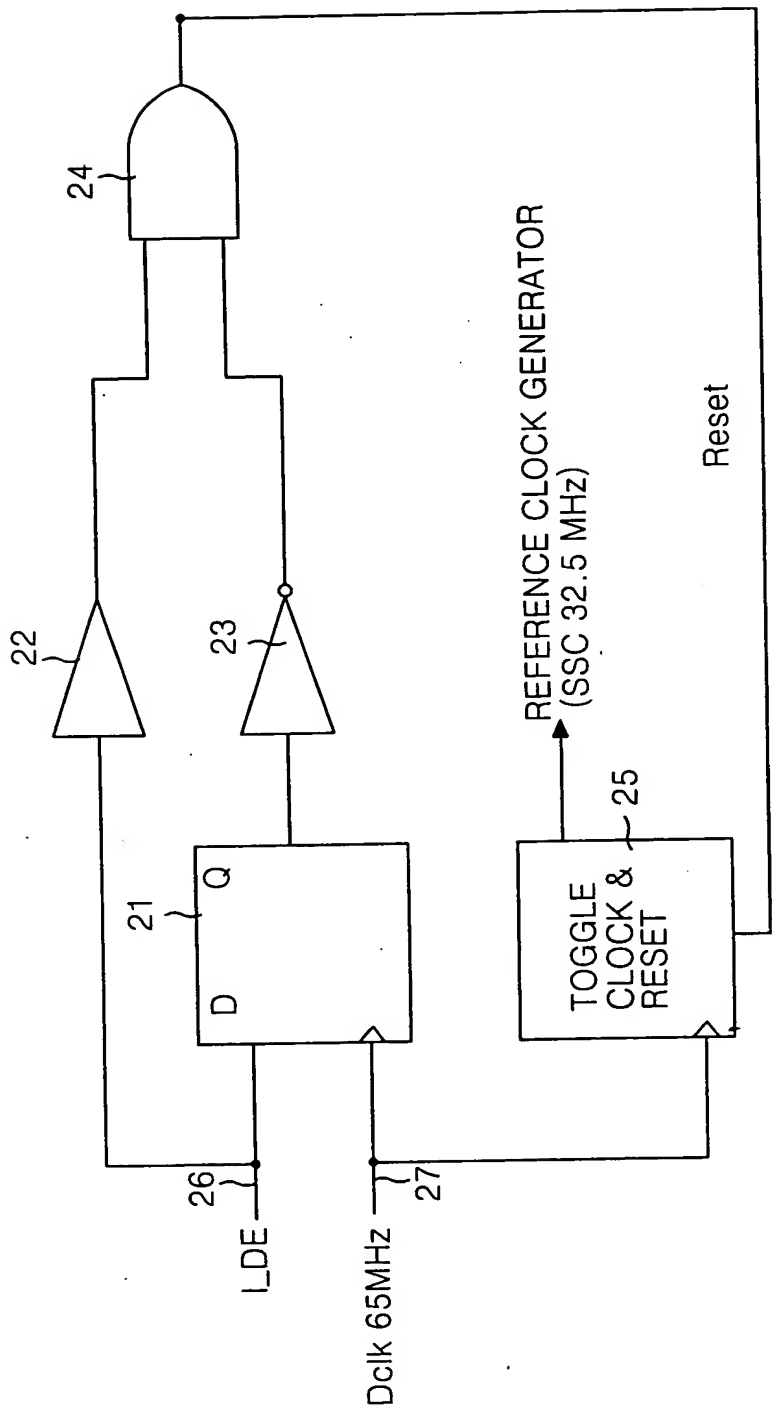
24
22
23
21
Q
D
25
TOGGLE
CLOCK &
RESET
REFERENCE CLOCK GENERATOR
(SSC 32.5 MHz)
Reset
26
27
I_DE
Dclk 65MHz

FIG.8

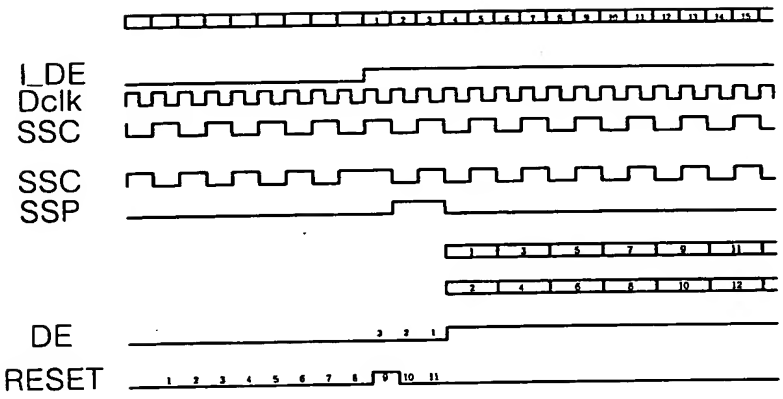

FIG.9A

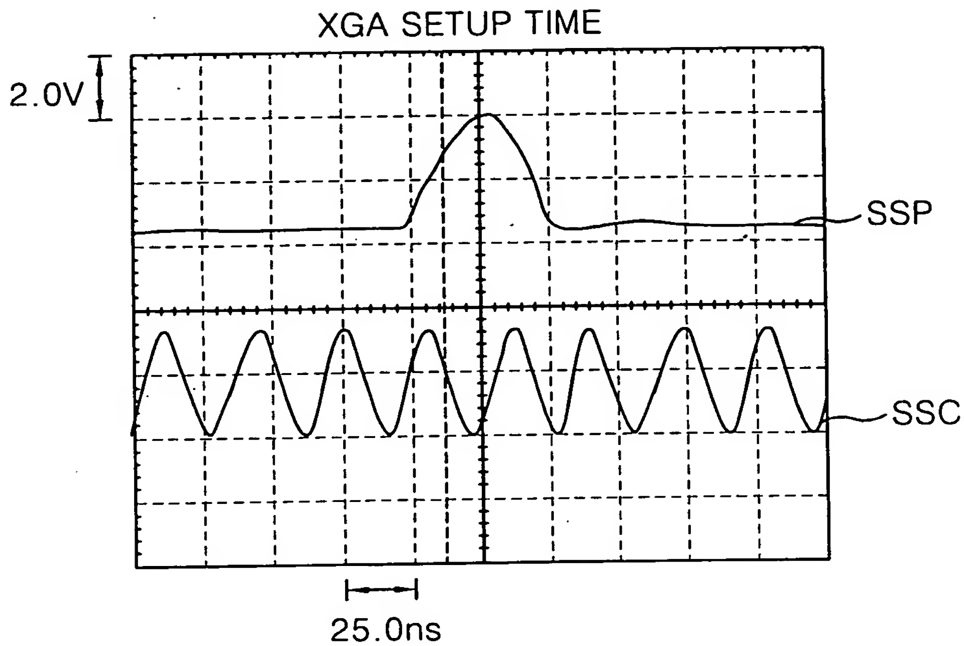

FIG.9B

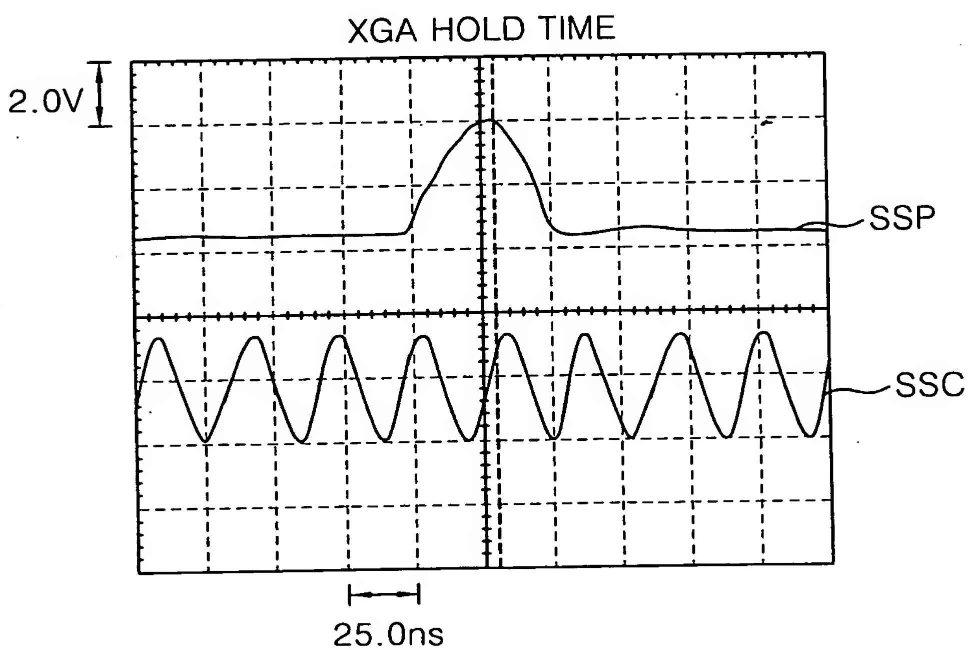

FIG.10A

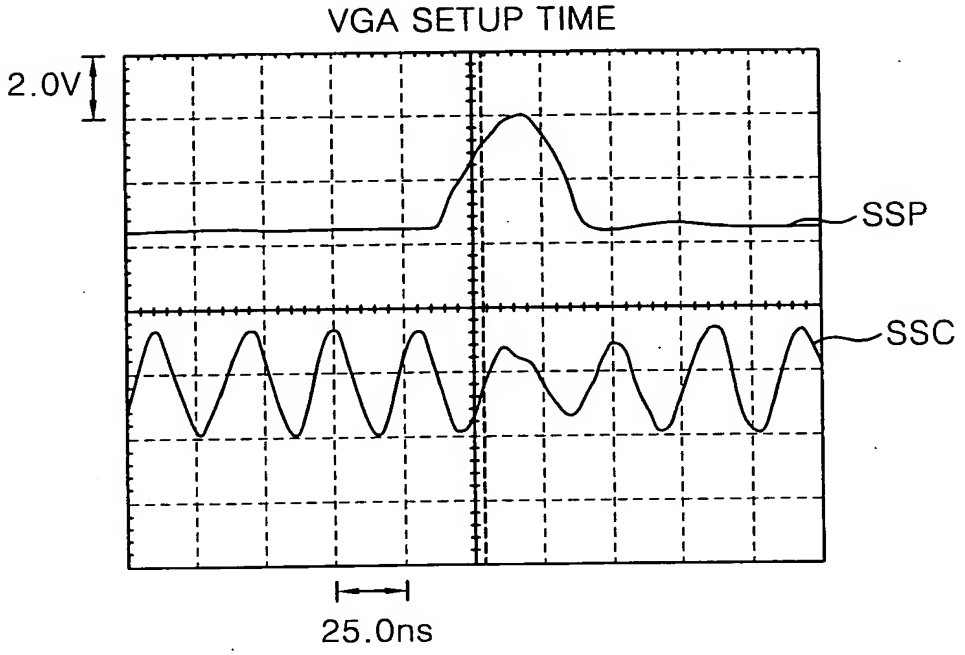

FIG.10B

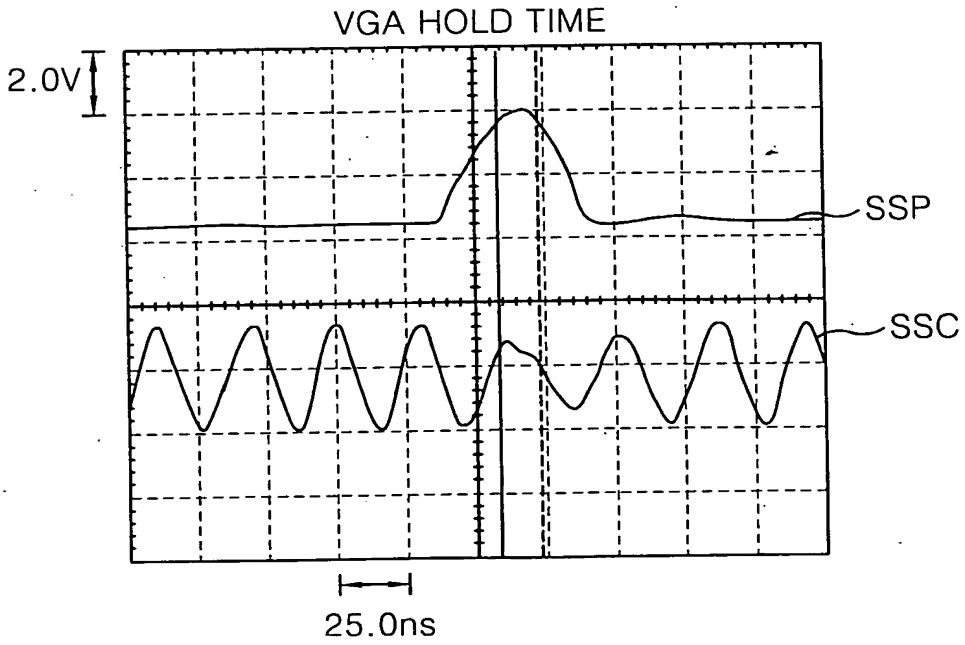

FIG.11A

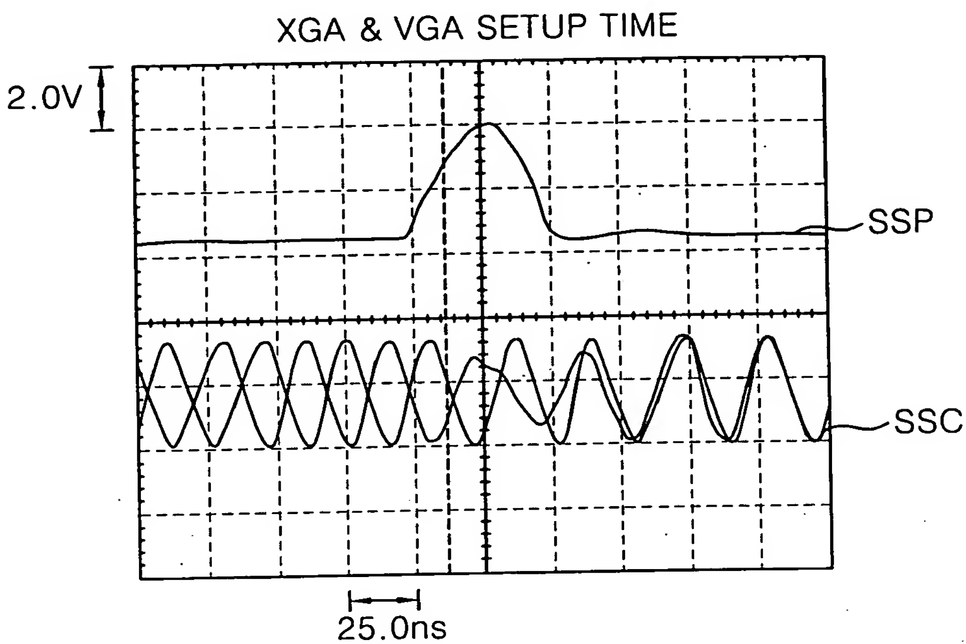

FIG.11B